**CLAIMS:**

1. A method of predistorting a signal, said method comprising:

producing sample output values each of which is dependent on one of a plurality of time spaced input samples and independent of any other time spaced input sample; and

combining said sample output values to produce a predistorted signal.

2. The method of claim 1 comprising:

retaining successive input signal samples as said time spaced input samples.

3. The method of claim 1 wherein producing each of said sample output values includes:

taking an absolute value of a time spaced sample;

using said absolute value as a pointer to a look-up table to produce an intermediate value; and

multiplying said intermediate value and said time spaced sample.

4. The method of claim 3 wherein said combining including:

adding said sample output values.

5. The method of claim 1 wherein said predistortion circuitry produces said predistorted signal, given a current input sample $u_n$, according to:

$$= u_n \bullet \sum_{k=0}^{K_0} c_{0k} \left|u_n\right|^k + u_{n-1} \bullet \sum_{k=0}^{K_1} c_{1k} \left|u_{n-1}\right|^k + \ldots + u_{n-L} \bullet \sum_{k=0}^{K_L} c_{Lk} \left|u_{n-L}\right|^k ,$$

where L is the maximum sample delay.

6. A predistortion system comprising:

predistortion circuitry adapted to produce sample output values each of which is dependent on one of a plurality of time spaced input samples and independent of any other time spaced input sample, and to combine said sample output values to produce a predistorted signal.

7. The system of claim 6 wherein said predistortion circuitry configured to retain successive input signal samples as said time spaced input samples.

8. The system of claim 6 wherein said predistortion circuitry configured, for producing each of said sample output values, to take an absolute value of a time spaced input sample, to use said absolute value as a pointer to a look-up table to produce an intermediate value, and to multiply said intermediate value and said time spaced input sample.

9. The system of claim 8 wherein said predistortion circuitry adapted to add said sample output values.

10. The system of claim 6 wherein said predistortion circuitry configured to produce said predistorted signal, given a current input sample $u_n$ , according to:

$$= u_n \bullet \sum_{k=0}^{K_0} c_{0k} \left| u_n \right|^k + u_{n-1} \bullet \sum_{k=0}^{K_1} c_{1k} \left| u_{n-1} \right|^k + \ldots + u_{n-L} \bullet \sum_{k=0}^{K_L} c_{Lk} \left| u_{n-L} \right|^k ,$$

where L is the maximum sample delay.